

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
(CASE NO. 13398US02)

Applicant:	Alexander G. MacInnis, et al.	<i>Electronically Filed on January 23, 2009.</i>
Application No.:	10/786,195	
Filed:	February 25, 2004	
For:	SIMD SUPPORTING FILTERING IN A VIDEO DECODING SYSTEM	
TC/A.U.	2193	
Examiner:	David H. Malzahn	
Conf. No.:	2398	

REPLY BRIEF

MS: APPEAL BRIEF-PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Appellant submits this Reply Brief in response to the Examiner's Answer mailed on November 25, 2008.

Appellant stands by the arguments made in the Appeal Brief. Appellant further responds below to select assertions made by the Examiner in the "Response to Argument" section of the Examiner's Answer.

On pages 3-4 of the Examiner's Answer, the Examiner asserts, "Wu's multi-port memory may be view (sic) as being multiple memory units because the plurality of data that is stored in M is stored in a plurality of storage locations or memory units." Appellant submits that this position is untenable and would lead to the conclusion that any memory unit is in fact multiple memory units, because all memory units have within them multiple memory locations. The term

“memory unit,” as it is understood by those in the art, and as it is described in the present specification, means more than just a memory location within a memory unit. The present claims refer not to “first and second memory locations,” but to “first and second memory units.” The multiport memory M of Wu, as described in the specification of Wu, and as would be understood by one of skill in the art, is one memory unit, not multiple memory units. The fact that the multiport memory M contains multiple memory locations does not change the fact that it is still a single memory unit.

On page 4 of the Examiner’s Answer, the Examiner asserts, “Also, associating an output port with M defines one memory unit and associating another output with M defines another memory unit.” Appellant respectfully disagrees. Just because a memory unit has two output ports does not make that memory unit two memory units.

On page 4 of the Examiner’s Answer, the Examiner asserts, “Wu’s shift registers shift their contents by a predetermined number of bits corresponding to the size of a data element when they receive the shift/load control signal 1, note column 3, lines 37-38.” Appellant respectfully disagrees. Claim 10, for example, says that the first and second shift registers “selectively shift (their) contents by a predetermined number of bits corresponding to the size of a data element.” This aspect of claims 10 and 19 is described in the specification at, for example, paragraph [0049], lines 7-10. In an illustrative embodiment of the invention, the data element is a pixel, and the shift registers Z0 and Z1 “shift left or right by a number of bits corresponding to the number of bits used to represent one pixel. In the illustrative embodiment described herein, a pixel is represented as a 16-bit value. Thus Z0 and Z1 have the ability to shift left or right by one word of 16 bits.” Paragraph [0049], lines 7-10. The shift registers rs21 and rs11 of Wu, on the other hand, are not described to shift by a *predetermined* number of bits, let alone by a predetermined number of bits that corresponds to the size of a data element. In fact, the operation of the shift registers rs21 and rs11 are not described in any detail in Wu. But in any event, the shift registers rs21 and rs11 are not described to shift by a *predetermined* number of bits *corresponding to the size of a date element* per claims 10 and 19.

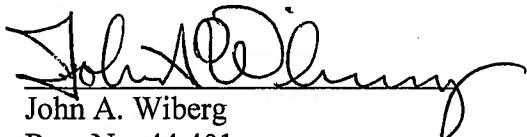
Appellant respectfully submits that claims 1-27 are allowable. Reversal of the Examiner’s rejection and issuance of a patent on the application are therefore requested.

Appl. No. 10/786,195
Reply Brief dated January 23, 2009

The Commissioner is hereby authorized to charge additional fee(s) or credit overpayment(s) to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Date: January 23, 2009

Respectfully submitted,



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